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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,383	04/19/2000	Stephen L. Willis	MICRON.092CP1	3147

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER

DIAZ, JOSE R

ART UNIT PAPER NUMBER

2815

DATE MAILED: 11/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/552,383

Applicant(s)

WILLIS, STEPHEN L.

Examiner

José R Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 30-37 and 56-62 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 30-37 and 56-62 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 30-32, 34 and 37 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Pat. No. 6,107,191) in view of Sandhu et al. (US Pat. No. 5,069,002). See Office action mailed on March 14, 2002.

➤ Claims 33 and 35-36 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Pat. No. 6,107,191) in view of Sandhu et al. (US Pat. No. 5,069,002), and further in view of Többen et al. (US Pat. No. 6,103,456). See Office action mailed on March 14, 2002.

➤ Claims 56-58 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Pat. No. 6,107,191) in view of Sandhu et al. (US Pat. No. 5,069,002).

Regarding claims 56-58, Han, as stated before, teaches a method of forming a semiconductor device (see cols. 1-6) comprising the steps of: forming a dielectric (230,240) (see Fig. 2A); forming a shield layer (235) (see Fig. 2A); forming a sacrificial layer (245) (see Fig. 2A); depositing a conductive material (270) (see Fig. 2G);

removing the conductive material (270) and the sacrificial layer (245) by using CMP process (see Fig. 2H and col. 1, lines 54-56). However, Han is silent with respect to the limitations of selecting an etchant and detecting when the CMP process has removed the sacrificial layer. Sandhu et al. teach that it is well known in the art to select an etchant and perform a sensing step during the CMP process, in which the change in friction is detected by rotating the wafer and polishing surfaces with electric motors and measuring current changes on one or both of the motors (see abstract and col. 3, lines 38-41 and 55-63 and col. 4, lines 28-30). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Han to select an etchant and to include a sensing step during the CMP process, in which the change in friction is detected by rotating the wafer and polishing surface with electric motors and measuring current changes on one or both of the motors. The ordinary artisan would have been motivated to modify Han in the manner described above for at least the purpose of producing a signal to operate control means for adjusting or stopping the process.

Regarding claim 62, Han further teaches the step of forming a cavity (250,255) in the dielectric layer (see Fig. 2F) and wherein depositing the conductive material (270) on the sacrificial layer (245) results in the cavity being filled with the conductive material (see Figs. 2G-2H).

➤ Claims 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Pat. No. 6,107,191) in view of Sandhu et al. (US Pat. No. 5,069,002), and further in view of Többen et al. (US Pat. No. 6,103,456).

Regarding claims 59-61, a further different between the claimed invention and the reference is the composition of each layer in the device. Han provides a general teaching of using any dielectric materials as the dielectric layer, the shield layer and the sacrificial layer (see col. 5, lines 25-37). Többen et al. teach that is well known in the art to use a DARC or nitride material as the shield layer (41) (see col. 11, lines 17-20) and an oxide layer as the sacrificial (42) (see col. 13, lines 4-8) and/or as a layer (23) under the shield layer (see col. 1, lines 20-31 and col. 8, lines 24-26). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to further modify Han to select an etchant and to include the use of DARC, nitride, and/or BPSG as the dielectric materials. The ordinary artisan would have been motivated to further modify Han in the manner described above for at least the purpose of providing protective layers with different etch rates.

Response to Arguments

➤ Applicant's arguments filed August 20, 2002 have been fully considered but they are not persuasive. Applicant argues that the reference Han fail to teach the CMP process and thus, there would be no motivation to combine this reference with the others used in the last Office action. However, the Examiner disagrees. Han, as acknowledged by Applicant in the remarks, teaches the use of a well known "planar

etch process" to remove the conductive material (270) and the sacrificial layer (245) (see Figures 2G-2H and col. 6, lines 13-16). Please note that the shield layer (235) remains on the structure after the planarization step (see Figs. 2G-2H). Further, Han incorporates the teaching of the reference S. Wolf ("Silicon Processing for the VLSI Era", Vols. I, II and III, Lattice Press) to clarify any confusion with any well-known term used in the disclosure, such as "conventional planar etch process" (see col. 1, lines 54-56). For example, S. Wolf ("Silicon Processing for the VLSI Era", Vol. II, Lattice Press, 1990, pp.238-239) clearly identifies the CMP as one of the very well known planar processes (see attachment). Thus, Han clearly anticipates the claimed invention since, as stated before, provides the teaching of the use of, for example, a CMP process to remove the conductive material and the sacrificial layer.

With regards to the reference Sandhu et al., Applicant should note that such a reference is not limited to any structure or method as argued by Applicant. As a matter of fact, Sandhu et al. is directed toward "a novel method and apparatus for detecting a planar endpoint in a semiconductor wafer during mechanical planarization" (see col. 1, lines 10-13). In other words, the teaching of Sandhu et al. can be applied to any structure in which a CMP process is needed. Thus, the teaching of Sandhu et al. can be used to modify the teachings of Han. Please note that the motivation can be found in the Abstract of Sandhu et al. Therefore, as made clear in the last Office action, the references Han and Sandhu et al. are combinable because first, they are from the same field of endeavor and second, a motivation was provided to combine the references. As such, the rejection is considered to be proper.

Conclusion

➤ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references disclose a method in which a CMP is used during the process of forming an inlaid capacitor (see paragraph [0032] of Amico et al. (US 2001/0014498 A1); col. 5, lines 58-60 and col. 7, lines 10-15 of Sandhu et al. (US Pat. No. 6,249,019 B1); and col. 5, lines 5-10 and col. 6, lines 33-35 of Tsai; and col. 6, lines 49-63 of Shih et al.) Furthermore, the reference Jang et al. (US Pat. No. 6,200,875 B1) discloses CMP of polysilicon plug using a silicon nitride stop layer.

➤ **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

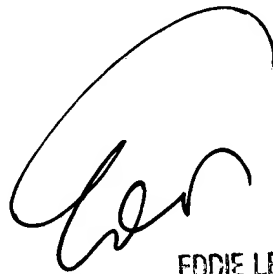
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-

6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
October 28, 2002



EDDIE LEE
SUPERVISOR, PATENT EXAMINER
TECHNOLOGY CENTER 2800